CLAIMS

1. A process for manufacturing a memory array formed of a plurality of stacked cells, comprising:

making a plurality of MOS transistors in respective active areas of a substrate made of semiconductor material, said step of making a plurality of MOS transistors comprising the steps of making, for each one of said MOS transistors, a first and a second conductive region in the substrate and a control electrode;

forming an insulating layer above the substrate;

for each MOS transistor, forming first and second electrical contacts extending through the insulating layer, the first and second electrical contacts being positioned directly above and contacting the first and second conduction regions, respectively;

making a plurality of capacitors, a corresponding one for each one of said MOS transistors, above said active regions, said step of making a plurality of capacitors comprising the steps of making, for each one of said capacitors, a first plate directly above and in contact with the first electrical contact of the corresponding MOS transistor, a dielectric material region above said first plate, and a second plate above said dielectric material region, each of the cells including one of the MOS transistors and a corresponding one of the capacitors;

making a plurality of bit lines connected to said second conductive regions of said MOS transistors by the second contacts; and

making a plurality of word lines and a plurality of plate lines running parallel to each other and perpendicular to said bit lines, each word line being connected to respective control electrodes of said MOS transistors and each plate line being connected to respective second plates;

wherein said step of making a dielectric material region comprises the step of making a same dielectric region shared by two adjacent cells in a direction parallel to said bit lines, and said step of making second plates of the capacitors comprises the step of making a

same third conductive region shared by the two adjacent cells in a direction parallel to said bit lines.

2. The process according to claim 1, wherein making a plurality of capacitors comprises:

depositing a first conductive material layer;

defining said first conductive material layer to form said first plates of said capacitors;

depositing a dielectric material layer on said first plates of said capacitors;

depositing a second conductive material layer on said dielectric layer;

sequentially etching said second conductive material layer and said dielectric material layer using a same mask, to form said same third conductive region and said same dielectric region, respectively.

3. The process according to claim 2 wherein said same third conductive region is aligned to said same dielectric region.

4. The process according to claim 2 wherein said same third conductive region has the same width as said same dielectric region, in said direction parallel to said bit lines.

5. The process according to claim 1, wherein said first plates of said capacitors form lower plates and said same dielectric region runs above and between the lower plates of said two adjacent cells.

6. The process according to claim 5, wherein said same dielectric region runs also on sides not facing each other of said lower plates of said two adjacent cells.

7. The process according to claim 1, further comprising forming a thick oxide layer that separates the MOS transistors of said two adjacent cells, wherein said same dielectric region and said same third conductive region run above said thick oxide layer.

8. The process according to claim 1, further comprising shaping said same dielectric region and said same third conductive region as respective elongated bands running perpendicular to said bit lines.

9. The process according to claim 1 wherein said bit lines run above said capacitors, and said same dielectric region forms a continuous layer except for openings corresponding to said contact regions.

11. The process according to claim 1 wherein said dielectric material region is made of ferroelectric material.

12. A process for forming a memory array, comprising:

forming a first stacked cell by forming a first transistor in a first active region of a semiconductive substrate and forming a first capacitor above the first active region, the first capacitor having a first and a second plate separated by a first dielectric region;

forming a second stacked cell by forming a second transistor in a second active region of the substrate and forming a second capacitor above the second active region, the second capacitor having a first and a second plate separated by a second dielectric region that is continuous with the first dielectric region, the second plate of the second capacitor being continuous with the second plate of the first capacitor; and

forming a third stacked cell by forming a third transistor in a third active region of the substrate and forming a third capacitor above the third active region, the third capacitor having a first and a second plate separated from each other by a third dielectric region that is continuous with the first and second dielectric regions, the second plate of the third capacitor

being continuous with the second plates of the first capacitor and the second capacitor, the first and second capacitors being positioned in a first directional line that is transverse to a second directional line in which the second and third capacitors are positioned.

13. The process of claim 12 wherein each of the first and second transistors includes first and second conductive regions and a control region and the first plates of the first and second capacitors are coupled to the first conductive regions of the first and second transistors, respectively.

14. The process of claim 12, wherein forming the first, second, and third capacitors includes depositing a first layer of conductive material; defining said first layer of conductive material to form said first plates of said capacitors; depositing a layer of dielectric material above said first plates; depositing a second layer of conductive material above said layer of dielectric material; defining said second layer of conductive material and said layer of dielectric material using a same mask to form said continuous second plates of said first, second, and third capacitors and said continuous first, second, and third dielectric regions.

15. The process of claim 12, wherein the second plates of the first, second and third transistors are part of a same plate line extending along the second directional line, further comprising shaping the first, second and third dielectric regions as a continuous elongated band running in parallel to the plate line.

16. The process of claim 12, further comprising forming a bit line connected to a conduction region of one of the first and second transistors, the bit line extending above the first and second capacitors along the first directional line.

17. A memory array, comprising:

a plurality of stacked cells, each cell including:

a MOS transistor formed in an active region of a substrate of semiconductor material;

a capacitor formed above said active region, each of said MOS transistors having a first and a second conductive region and a control electrode and each of said capacitors having a first and a second plate separated by a dielectric material region; said first conductive region of each of said MOS transistors being connected to said first plate of a respective capacitor;

a plurality of bit lines connected to said second conductive regions of said MOS transistors of respective cells of the plurality of stacked cells;

a plurality of word lines connected to said control electrodes of respective said MOS transistors of the plurality of stacked cells;

a plurality of plate lines connected to said second plate of respective said capacitors, said plate lines running perpendicular to said bit lines and parallel to said word lines;

wherein a pair of cells adjacent to each other in a direction parallel to said bit lines share a same dielectric material region and a same third conductive region, forming said second plates of said capacitors of said pair of cells.

18. The memory array according to claim 17, wherein said first plates of said capacitors form lower plates and said same dielectric material region runs above and between the lower plates of said two adjacent cells.

19. The memory array according to claim 18, wherein said same dielectric material region runs also on sides not facing each other of said lower plates of said two adjacent cells.

20. The memory array according to claim 17, wherein said same dielectric material region is shaped as a band running in parallel to said respective plate line.

21. The memory array according to claim 17, wherein said same third conductive region is positioned on and coextensive with said same dielectric region.

22. The memory array according to claim 21, wherein said same third conductive region has the same width as said same dielectric region, in said direction parallel to said bit lines.

23. The memory array according to claim 17, wherein said dielectric material region is made of ferroelectric material.

24. A memory array, comprising:

a substrate of semiconductor material;

a first stacked cell comprising a first transistor formed in a first active region of the substrate and a first capacitor formed above the first active region, the first capacitor having a first and a second plate separated by a first dielectric region;

a second stacked cell comprising a second transistor formed in a second active region of the substrate and a second capacitor formed above the second active region, the second capacitor having a first and a second plate separated by a second dielectric region that is continuous with the first dielectric region, the second plate of the second capacitor being continuous with the second plate of the first capacitor; and

a third stacked cell comprising a third transistor formed in a third active region of the substrate and a third capacitor formed above the third active region, the third capacitor having a first and a second plate separated from each other by a third dielectric region that is continuous with the first and second dielectric regions, the second plate of the third capacitor being continuous with the second plates of the first capacitor and the second capacitor, the first and second capacitors being positioned in a first plane that is transverse to a second plane in which the second and third capacitors are positioned.

25. The memory array according to claim 24, wherein said first plates of said capacitors form lower plates and said dielectric regions are part of a dielectric layer that runs above and between the lower plates of said capacitors.

26. The memory array according to claim 25, wherein said dielectric layer runs also on sides not facing each other of said lower plates of said capacitors.

27. The memory array according to claim 24, wherein said dielectric regions are part of a dielectric layer that is shaped as a dielectric band extending in a first direction and the second plates are part of a plate line extending in the first direction in parallel to said dielectric band.

28. The memory array according to claim 24, wherein said conductive band is positioned on and coextensive with said dielectric band.

29. The memory array according to claim 24, wherein said dielectric regions are made of ferroelectric material.